520.44579X00

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Yoshinobu TARUTANI et al.

Serial No.:

(not yet assigned)

Filed:

December 30, 2004

For:

Superconducting Driver Circuit

## INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97 & 1.98

December 30, 2004

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

In the matter of the above-identified application, applicant(s) are submitting herewith a copy of the documents listed in the attached form equivalent to Form PTO-1449 for the Examiner's consideration.

This information disclosure statement is being submitted with the new application.

To the extent that the documents listed on the attached form equivalent to Form PTO-1449 are not in the English language, the requirement of 37 CFR 1.98(a)(3) for a concise explanation of the relevance is satisfied by

an English Abstract and/or the discussion of these documents in the specification.

It is respectfully requested that this information disclosure statement be considered by the Examiner.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135  $^{\circ}$  5  $^{\circ}$  9  $^{\circ}$  5  $^{\circ}$  9 (520.44579X00) and please credit any excess fees to such deposit account.

Respectfully submitted,

Melvin Kraus

Registration No. 22,466

ANTONELLI, TERRY, STOUT & KRAUS, LLP

MK/anp Attachments (703) 312-6600 6

of

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Substitute for form 1449A/PTO Complete if Known / 5 1971

## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Sheet

	Complete if Known : 1 🤭 L 🦞 📗 🖫
Application Number	
Filing Date	December 30, 2004
First Named Inventor	Yoshinobu TARUTANI, et al.
Art Unit	
Examiner Name	
Attorney Docket Number	520 44570Y00

U.S. PATENT DOCUMENTS					
Examiner Initials'	Cite No. <sup>1</sup>	Document Number  Number-Kind Code <sup>2</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS						
Examiner Initials'	Cite No.1	Foreign Patent Document  Country Code <sup>3</sup> -Number <sup>4</sup> -Kind Code <sup>5</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	7
		2000-261307	09/22/2000	JAPAN		
		2001-068995	03/16/2001	JAPAN		
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				]		

Examiner	Date	
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no persons are required to respond to a collection of information unless it displays a valid OMB control number. Under the Paperwork Reduction Act of Substitute for form 1449/PTO Complete if Known **Application Number** INFORMATION DISCLOSURE Filing Date **December 30, 2004** STATEMENT BY APPLICANT First Named Inventor Yoshinobu TARUTANI, et al. Group Art Unit (use as many sheets as necessary) Examiner Name Sheet of Attorney Docket Number 520-44579X00

		NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		H. Suzuki et al. "Applications of Synchronized Switching in Series-Parallel-Connected Josephson Junctions", IEEE Transactions on Electron Devices, vol. 37, p.2399, 1990 *cited in the specification on pge 4 and the search report of the PCT proceduce	
		O.A. Mukhanov et al. "Josephson Output Interfaces for RSFQ Circuits", IEEE Transactions on Applied Superconductively, vol. 7, p. 2826, 1997 cited in the specification on page 2	
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Examiner	Date	
Signature	Considered	

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